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STUDY OF ELECTRICAL CHARACTERISTIC OF NEW P-TYPE TRENCHED UMOSFET

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ABSTRACT
In this paper p-type trenched UMOSFET was designed without super junction and constructed like any other conventional MOSFET. Characteristic curve was studied between drain current verses drain voltage and drain current verses gate voltage. The trench was designed under TCAD simulation tool Silvaco software using etching process. The specific channel length of the p-type UMOSFET has been concentrated as 0.9 microns. The device structures are designed using Silvaco Athena and characteristics were examined using Silvaco Atlas.

INTRODUCTION
In the year 1991 first trench U-shape MOSFET was reported by Cree Inc. [1]. The UMOSFET is a vertical or trench structure in MOS transistor. The trench was done by etching techniques developed for storage capacitor used in silicon memories [1]. It offers significant advantages in speed and lowers the ON resistance. As a result manufacturers are offering trench or vertical form of structure for MOS transistor in electronic components [2]. It has been developed for DRAMs. Since the specific on-state resistance of the UMOSFET structure is smaller than DMOSFET. This structure allows further reduction of the specific on-resistance [3]. In order to modulate the electric field of the drift region and electric field peaks at the side wall junction between p-pillar and n-drift region a split-gate resurf stepped oxide (RSO) vertical UMOSFET with p-pillar structure was proposed [4]. Also the trench MOS technology is widely used for power management [5]. An improved UMOS with ultra-low specific on-resistance which uses a self-aligned process that increases channel density and therefore, reduces on-resistance per unit area of the TC-UMOS which is more effective than source contact UMOS for reducing on-state resistance by scaling down the cell pitch [6][7][8]. This short channel combines a simple U-groove geometry which investigate the breakdown voltage and on-resistance and same as VMOS, DMOS and UMOS vertical power devices [9][10]. The relationship between on-resistance and packing density can be calculated in the vertical power MOSFET with rectangular grooved MOS [11]. Due to the recent advancement in the power handling capability in power MOS transistor it is possible to achieve short active channel and can model the MOS resulting the on-resistance and device performance affected by silicon defects(interstitial and vacancy) induced by trench process due to the threshold voltage shift [12][13]. To overcome on-state specific resistance and breakdown voltage a gate-enhanced power UMOSFET with the deep trench polysilicon electrode contacted to gate electrode was designed, that maintains the breakdown voltage and forms high-electron current density which results in lower on-resistance [14]. Many hardening methods which can improve the SEB survivability [15] and to conduct a good forward characteristic with low forward voltage at high current density for a field-controlled MOS trench thyristor was proposed [16] [17] . Since the gate enhanced power UMOSFET with split gate reduces the specific on-resistance, it also reduces the gate source electrode parasitic capacitor [18][19]. However Silicon Carbide (SiC) an emerging semiconductor material being used for switching applications in the U-grooved MOS capacitor, it was found that the general appearance of capacitor-voltage curve was unchanged although the leakage of the oxide was increased [20][21]. Hence the sensitivity of the super junction MOSFET is high due to charge imbalance. A silicon super junction MOSFET of very low on-resistance and very low gate-to-drain switching is reported [22][23].

MATERIALS AND METHODS
The above structure shows the p-type U-shaped Trench MOSFET (UMOSFET) based on the orientation of p-type <100> wafer simulated in the area of 1x1µm. using Silvaco TCAD. The structure designing was done by ATHENA tool and electrical characteristics were obtained by ATLAS tool. The structure is designed like

conventional MOSFET, a groove is created in substrate by etching processing and gate contact is implanted in that groove. The structure so designed is a combination of U-groove and conventional MOSFET.

gate oxide=815.526 angstroms (0.0815526 um) X.val=0.5
pxj=0.883634 um from top of first Silicon layer X.val=0.1
p++ sheet rho=29.3262 ohm/square X.val=0.05
LDD sheet rho=23.2093 ohm/square X.val=0.3
chan surf conc=9.94396e+019 atoms/cm3 X.val=0.45
p1dvt=3.0849e+013 V X.val=0.49

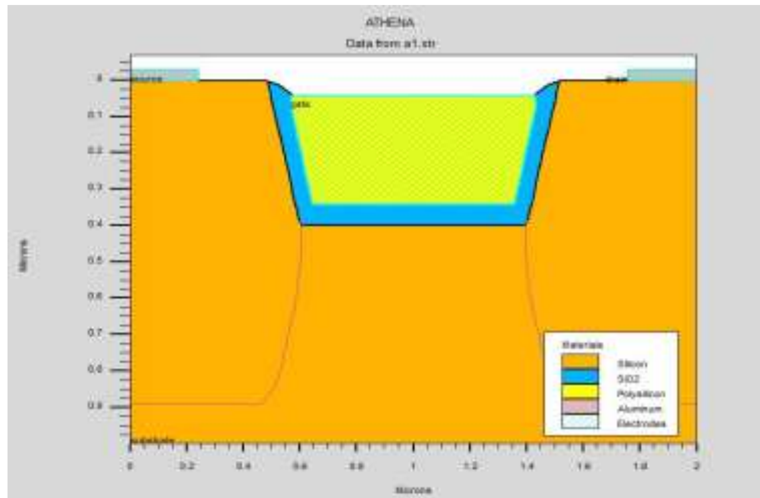

Fig1 Structure of Etched U-shape grooved gate UMOSFET

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RESULTS AND DISCUSSION

For etched U-shape grooved gate UMOSFET the curve between Drain current verses Drain Voltage is shown in fig 2 (a) at different values of Vgs= -1.1V, -2.2V and -3.3V. The curve between Drain Current verses Gate Voltage is shown in fig 2(b) at different values of Vds=-0.1V, -1.1V, -2.1V and -3.1V.

By applying drain voltage the drain current increases reaching to the maximum current and then it saturate. In fig 2(b) Id vs Vg graph shows different curves when gate voltage is applied. At first graph the voltage is in saturation and then it decreases down the current. In the second case voltage first decreases and then increases to the maximum current. In the third and fourth graph the voltage increases linearly and exponentially respectably.

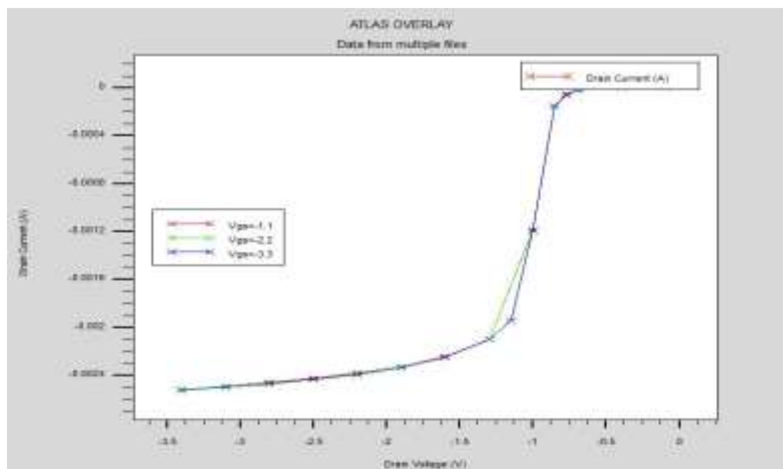

Fig 2(a) Cumulative for Drain Current and Drain Voltage

It was observed that at different values of V_{GS}, the value drain current when reaches at -0.0022A it becomes constant on increasing the drain voltage.

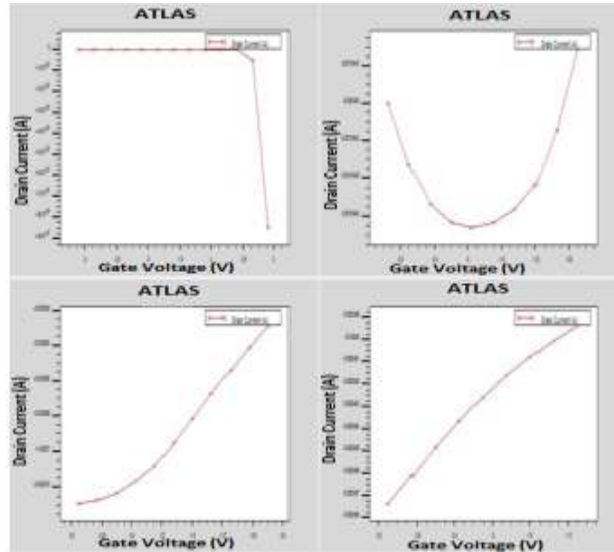

Fig2 (b). Cumulative for Drain Current and Gate Voltage

Hence MOSFET works in three regions,
Region 1: Cut-off region.
Region 2: Triode region.

$$I_D = \mu_n C_{ox} \frac{W}{L}((V_{\{GS\}} - V\{th\})V_{\{DS\}} - \frac{V_{\{DS\}}^2}{2}) \quad (1)$$

Region 3: Saturation region

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda(V_{DS} - V_{DSsat})) \quad (2)$$

Where,
μ_n= electron mobility
C_{ox}= oxide capacitance per unit area
W= gate width
L= gate length
λ= channel length modulation
The output can be observed from given tables for design parameters and for current and voltage values for etched U-shape grooved gate MOSFET.

Table 1. For Design Parameters

S.No.	For Design Parameters	
		Etched U-shape grooved UMOSFET (p-type)
1	Gate Oxide	815.526 angstroms(Å)
2	Junction thickness	0.883634 (μm)
3	Threshold voltage	3.0849e+013 (V)
4	Resistance	29.3262 (ohm/square)
5	LDD resistance	23.2093 (ohm/square)
6	Channel Length	0.9 μm

Table 2 (a) and (b) shows the curve between drain current verses drain voltage and drain current verses gate voltage for etched U-shape grooved UMOSFET

TABLE 2(A). FOR ETCHED U-SHAPE GROOVED UMOSFET THE VALUES OF DRAIN CURRENT AND DRAIN VOLTAGE CAN BE OBSERVED AS

	(A) For Drain Current and Drain Voltage					
	Vg=-1.1		***Vg=-2.2***		***Vg=-3.3***	
S.No.	***Vd(V)***	***Id(A)***	***Vd(V)***	***Id(A)***	***Vd(V)***	***Id(A)***
1	-0.1	0	-0.1	0	-0.1	0
2	-0.4	0	-0.4	0	-0.4	0
3	-0.7	0	-0.7	-0.0001	-0.7	0
4	-0.85	-0.0001	-1	-0.0012	-0.85	-0.0001
5	-1.3	-0.0021	-1.3	-0.0021	-1.3	-0.0021
6	-1.6	-0.0022	-1.6	-0.0022	-1.6	-0.0022
7	-1.9	-0.0023	-1.9	-0.0023	-1.9	-0.0023
8	-2.2	-0.00239	-2.2	-0.00239	-2.2	-0.00239
9	-2.5	-0.0024	-2.5	-0.0024	-2.5	-0.0024
10	-2.8	-0.00245	-2.8	-0.00245	-2.8	-0.00245
11	-3.1	-0.00249	-3.1	-0.00249	-3.1	-0.00249
12	-3.4	-0.0025	-3.4	-0.0025	-3.4	-0.0025

TABLE 2(B). FOR ETCHED U-SHAPE GROOVED UMOSFET THE VALUES OF DRAIN CURRENT AND GATE VOLTAGE CAN BE OBSERVED AS

	(B) For Drain Current and Gate Voltage							
	Vd=-0.1		***Vd=-1.1***		***Vd=-2.1***		***Vd=-3.1***	
S.N0.	***Vg(V)***	***Id(A)***	***Vg(V)***	***Id(A)***	***Vg(V)***	***Id(A)***	***Vg(V)***	***Id(A)***
1	-3.25	0	-2.95	-0.001842	-3.1	-0.002373	-3.1	-0.0024975
2	-3	0	-2.7	-0.00184265	-2.95	-0.0023727	-2.85	-0.0024963
3	-2.75	0	-2.45	-0.0018431	-2.35	-0.0023725	-2.6	-0.002495
4	-2.49	0	-2.2	-0.0018433	-2.6	-0.0023717	-2.35	-0.0024937
5	-2.25	0	-1.95	-0.00184335	-2.1	-0.002371	-2.1	-0.0024927
6	-2	0	-1.7	-0.0018433	-1.85	-0.0023695	-1.85	-0.0024917
7	-1.25	0	-1.45	-0.00184315	-1.6	-0.002368	-1.6	-0.002491
8	-1.5	0	-1.2	-0.0018429	-1.35	-0.002367	-1.35	-0.002492
9	-1.15	0	-0.95	-0.0018423	-1.0	-0.0023655	-1.1	-0.0024895
10	-1	0	-0.7	-0.00184135	-0.85	-0.002364		
11	-0.25	0			-0.6	-0.002363		
12	-0.5	0						
13	-0.025	$-2x10^{-7}$						
14	0	$-1.3x10^{-6}$						

It was observed that for different values of V_{ds} it resulted variations in drain current and gate voltage.
For V_d=-0.1V drain current remains zero and increases at V_g=-0.025V.
For V_d=-1.1V, -2.1V and -3.1V drain current remains slightly constant and becomes zero at voltage above V_g=-0.5.
ATLAS output for threshold voltage of p-type trenched UMOSFET is extracted as below:
EXTRACT> #extract long chan vt
EXTRACT> extract name="p1dvt" 1dvt ptype qss=1e10 x.val=0.49
p1dvt=3.0849e+013 V X.val=0.49

CONCLUSION

This structure was designed like any other conventional MOSFET with no superjunction UMOSFET. It resulted that designing a new p-type trenched UMOSFET structure can attain the better performance parameters like trenched UMOSFET. It can be concluded that the reliability can be improved by p-type trenched UMOSFET without superjunction structure.

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